WHAT IS CLAIMED IS:

1. A method for testing a semiconductor device including first and second power source lines, a plurality of output circuits, and a plurality of output terminals each disposed for one of said output circuits, each of said output circuits including a combination of first and second transistors connected together in series via a first node and between said first power source line and said second power source line, said first node being connected to a corresponding one of said output terminals, said method comprising the steps of:

controlling said output circuits to turn ON said first and second transistors of a first output circuit among said plurality of output circuits and turn ON and OFF said first transistor and said second transistor, respectively, a second output circuit among said plurality of output circuits;

measuring a potential difference between said output terminal of said first output circuit and said output terminal of said second output circuit and a penetrating current flowing through said first and second transistors of said first output circuit; and

calculating a characteristic of said first or second transistor of said first output circuit based on said potential difference and penetrating current.

2. The method according to claim 1, wherein at least one of said first and second transistors includes a plurality of transistor elements connected in parallel, and a specified number of said transistor elements among said plurality of transistor elements are turned ON during said controlling step.

3. The method according to claim 1, further comprising the step of selecting arbitrary two of said plurality of output circuits as said first and second output circuits, before said controlling step.

4. The method according to claim 1, wherein said controlling step uses external pins of said semiconductor device to turn ON said first and second transistors of said first output circuit and to turn ON and OFF said first transistor and said second transistor, respectively.

5. The method according to claim 1, wherein said measuring step uses a constant current source connected between said first power source line and said second power source line.

6. A recording medium for storing therein a program for running a computer thereon to conduct the method according to claim 1.

7. A semiconductor device comprising:

first and second power source lines;

a plurality of output circuits including at least first and second output circuits, each of said output circuits including a combination of first and second transistors connected together in series via a first node and between said first power source line and said second power source line;

a plurality of output terminals each disposed for one of said output circuits, said first node being connected to a corresponding one of said

output terminals; and

a control circuit for controlling said output circuits during a test mode to turn ON said first and second transistors of said first output circuit, and turn ON and OFF said first transistor and said second transistor, respectively, of said second output circuit.

8. The semiconductor device according to claim 7, wherein said control circuit turn OFF said first and second transistors of said output circuits other than said first and second output circuits.

9. The semiconductor device according to claim 7, wherein said first and second transistors are p-ch and n-ch MIS transistors, respectively.

10. The semiconductor device according to claim 7, wherein at least one of said first and second transistors includes a plurality of transistor elements connected in parallel.

11. The semiconductor device according to claim 7, wherein said control circuit includes a decoder for decoding external signals to deliver a control signal for controlling said output circuits.

12. The semiconductor device according to claim 11, wherein said control signal selects a potential to be provided to control electrodes of said first and second transistors.

13. The semiconductor device according to claim 7, further comprising a functional circuit block connected between said first power source line and said second power source line, and a control switch for isolating said functional circuit block from said first or second power source line said test mode.

14. The semiconductor device according to claim 7, wherein said first and second output circuits are connected between said first power source line and said second power source line via a common branch line extending from said first or second power source line.